REMARKS

Applicant respectfully requests reconsideration and allowance of claims 1-17, 19 and 21-24 which are pending in the above-identified application.

Applicant's representatives thank the Examiner for granting the telephone interview of March 4, 1997 during which the substance of this amendment was discussed in detail.

Applicant has cancelled claims 18 and 20 and applicant has amended claims 5-6, 15 and 19. Applicant has added new claims 21-24. Applicant submits that the amendments made to claims 5-6, 15 and 19 and the subject matter of new claims 21-24 are fully supported by the specification, claims and drawing as originally filed.

In Part 2 of the Office Action, the Examiner rejected claim 6 under 35 U.S.C. §112, second paragraph as being indefinite contending that the term "control logic" was unclear. In response, applicant has amended claim 6 and removed the recitation of the term "control logic". Further claim 6 has been amended to more clearly recite that the integer data words received by the shift registers have a length of eight bits or multiples thereof. Accordingly, applicant submits that the Examiner's §112 rejection is overcome.

In Parts 3 and 4 of the Office Action, the Examiner rejected claims 5 and 20 under 35 U.S.C §102(b) as being anticipated by U.S. Patent No. 4,418,383 to Doyle (hereinafter "the Doyle reference"). The Examiner contended that the Doyle reference disclosed all of the features of the claimed invention. Applicant submits that the Examiner's rejection as to claim 20 is moot because applicant has cancelled the subject claim without prejudice. Applicant, however, traverses the Examiner's rejection of claim 5.

Amended claim 5 recites that "the word length of the arithmetic logic unit being automatically adjustable in accordance with the length of the integer data words being processed, the length of the integer data words being 8 bits or multiples thereof." The Doyle reference, however, does not

disclose this limitation. Indeed, the Doyle reference states that a component must be used "in a combination of identical part number components to provide data flow paths and functions of different data widths..." (col. 3, lines 5-13). Thus, the Doyle reference does not disclose a single ALU with an adjustable word length of eight bits or multiples thereof as recited in claim 5 of the instant application and, accordingly, the Examiner's §102 rejection should be withdrawn.

In Part 5 of the Office Action, the Examiner rejected claim 6 under 35 U.S.C. §102(b) as being anticipated by the Cook reference for the reasons set forth in the previous Office Action. Applicant respectfully traverses the Examiner's rejection. Specifically, the Cook reference does not disclose, among other limitations, a shift register unit capable of receiving an integer data word having a length **of eight bits or multiples thereof** as recited in claim 6 hereinabove. Therefore, the Cook et al. reference does not disclose every element of the claim. Indeed, during the telephone interview of March 4, 1997, the Examiner stated that the amendments made herein to claim 6 overcame the prior art of record. Thus, the Examiner's §102(b) rejection of claim 6 should be withdrawn.

In Parts 6 and 7 of the Office Action, the Examiner rejected claims 4 and 19 under 35 U.S.C. §103(a) as being unpatentable over the Birman reference in view of the Wong reference. The Examiner contended that the Birman reference did not disclose an adjustable word length multiplier but the Wong reference taught such a multiplier and, therefore, it would have been obvious to combine the teachings of the Birman and Wong references to obtain the claimed invention. Applicant respectfully traverses the Examiner's rejection.

Claims 4 and 19 recite that a single multiplier unit is capable of multiplying data having a length of eight bits or multiples thereof, which imparts great versatility to a system for processing digital data. Contrary to the Examiner's contention, the Wong reference does not disclose a multiplier unit capable of manipulating digital data words having a length

of eight bits or multiples thereof. Indeed, the Wong reference expressly states that "a multiplier which performs complex fixed and floating point arithmetic multiplications on a plurality of selected input words having a **predetermined data word length** (32 bits)." (Column 1, lines 57-61). Thus, the combination of the Birman reference and the Wong reference does not recite each and every feature as specified in claims 4 and 19 of the instant application.

During the telephone interview of March 4, 1997, the Examiner asserted that the Wong reference discloses a multiplier system capable of operating on digital data words having a length of either 32 or 16 bits (col. 2, line 34). Assuming, arguendo, that the Examiner is correct, that reference still does not disclose or suggest, alone or in combination with the Birman reference, the instant invention as recited in claims 4 and 19. Specifically, the Wong reference requires a plurality of multiplier units 14a, 14b, 382, 384, 386, and 388 to facilitate operating on data words of only 32 or 16 bits (col. 2, line 34; and Figs. 1 and 3). Thus, the combination cited by the Examiner does not teach or suggest a single multiplier with an adjustable word length of eight bits or multiples thereof as recited in claims 4 and 19 of the instant application. Accordingly, the Examiner's §103 rejection of claims 4 and 19 should be withdrawn.

In Part 8 of the Office Action, the Examiner rejected claims 1-3, 7-12 and 14-18 under 35 U.S.C. §103(a) as being unpatentable over the Birman reference in view of the Wong reference as applied to claims 4 and 19 and further in view of the Doyle reference. The Examiner contends that neither the Birman nor the Wong references teach adjustable word lengths in an ALU but the Doyle reference teaches the features of an ALU as claimed. Applicant respectfully traverses the Examiner's rejection.

As discussed above, the Wong reference does not teach a multiplier with an adjustable word length of eight bits or multiples thereof as recited in claims 4 and 19 of the instant application. Further, independent claims 1 and 15 also contain

the recitation that the data words of the multiplier unit have a length of eight bits or multiples thereof. The Doyle reference, however, does not cure this deficiency in the cited references. Indeed, the Doyle reference states that a component must be used "in a combination of identical part number components to provide data flow paths and functions of different data widths..." (col. 3, lines 5-13). Thus, the combination cited by the Examiner does not teach or suggest a single multiplier with an adjustable word length of eight bits or multiples thereof as recited in claims 1, 4, 15, 19 and new claim 21 of the instant application.

Applicant has reviewed Fig. 7 of the instant specification, as suggested by the Examiner during the telephone interview, and has determined that the multiplier, as recited in claims 1, 4, 15, 19 and new claim 21, does not represent a plurality of individual multipliers as disclosed by the Doyle reference. In reviewing the specification at page 6, line 31 to page 7, line 6; the User Manual v 2.80 at pages 127, 129 and 139; and Fig. 7, one skilled in the art would know that the multiplier as claimed is a single item and is merely schematically represented as multiple functional blocks in the figures of the specification. Accordingly, the multiplier as recited in claims 1, 4, 15, 19 and new claim 21 is neither disclosed nor suggested, alone or in combination, by the prior art of record.

Accordingly, each and every feature of the invention as recited in claims 1, 4, 15, 19 and new claim 21 is not suggested by the Birman reference in view of the Wong reference as applied to claims 4 and 19 and further in view of the Doyle reference. Thus, the Examiner's §103 rejection as to those claims should be withdrawn.

Further, claims 2, 3, 7-12 and 14 depend from claim 1 and contain all of the limitations thereof as well as other limitations. Still further, claims 16-18 and new claims 22-24 depend from claim 15 and contain all of the limitations of that claim. Therefore, the subject dependent claims are likewise

patentable for the reasons presented herein with regard to claims 1 and 15, respectfully, as well as other reasons.

In Part 8 of the Office Action, the Examiner set forth additional reasons for rejecting claims 2 and 7-18. However, for the reasons presented hereinabove, these claims are dependent on a clearly patentable base claim and claim 15 is a patentable independent claim. Accordingly, applicant submits that the subject claims are patentable over the cited art.

Applicant has added new independent claim 21 which further recites the details of the bus structure of the present invention. Specifically, claim 21 sets forth that the bus structure includes:

> a first bus coupled to an output of the multiplier unit for receiving the digital data words therefrom;
> a second bus coupled to an output of the arithmetic logic unit for receiving the digital data words therefrom;
> third and fourth busses coupled to outputs of the two registers, respectively, for receiving the digital data words therefrom; and
> a fifth bus coupled to the inputs of the multiplier unit, the arithmetic logic unit and the register unit for transmitting the digital data words thereto.

The above recited bus structure is not disclosed or suggested in the cited art of record and, therefore, claim 21 is clearly patentable over the prior art.

In light of the amendments made hereinabove, applicant believes that the instant claims are in condition for allowance. The Examiner is invited to contact the undersigned to discuss any still outstanding matters. Early and favorable action is earnestly solicited.

I hereby certify that this correspondence is being deposited with the United States Postal Service as first class mail in an envelope addressed to: Commissioner of Patents and Trademarks, Washington, D.C. 20231, on March 13, 1997

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Name of applicant, assignee or Registered Representative

Signature

March 13, 1997
Date of Signature

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Respectfully submitted,

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